

NANOARC

ACE Hardware and Operator-Panel Architecture Manual

Revision A.0 - Control-Module Hardware Baseline

AGC-inspired low-voltage control hardware for the Arduino Nano Every platform

ACE hardware partition and safety boundary

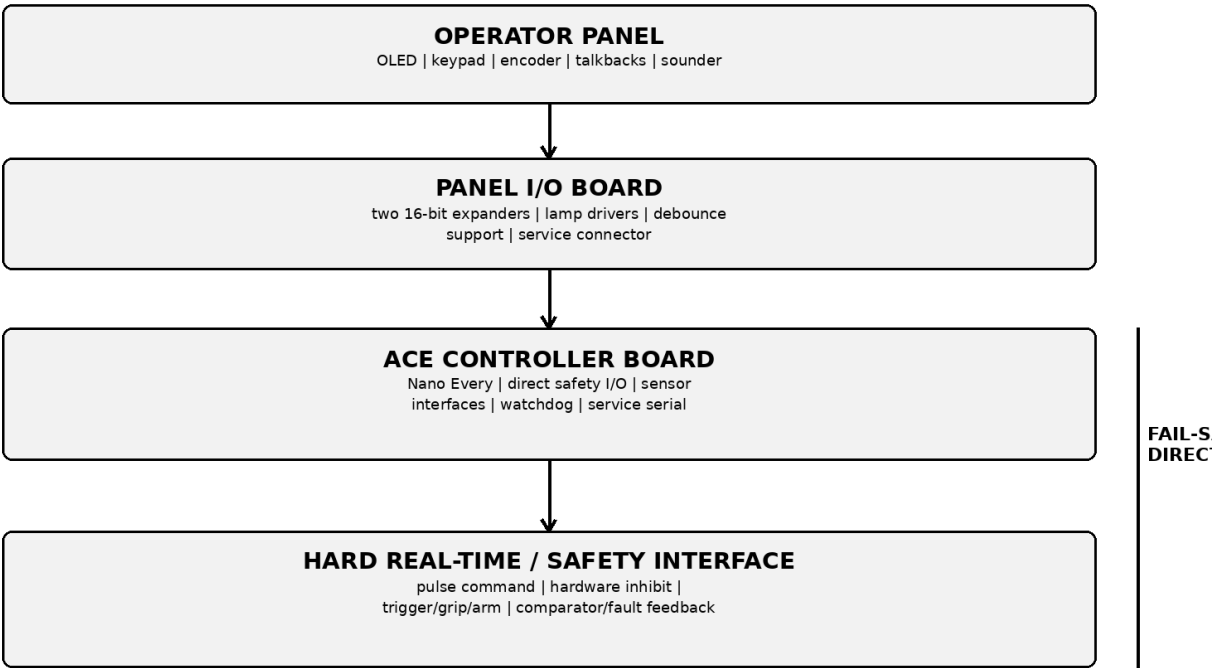


Figure 1. ACE hardware layers and the fail-safe boundary.

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Revision	A.0 / 0.1
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Status	Working hardware architecture baseline

DESIGN NOTE: This manual defines the low-voltage ACE controller, operator panel and interface hardware. It is not an energy-stage construction or operating procedure.

Document Control

Revision	Date	Status	Summary
0.1 / A.0	2026-06-24	Baseline	Initial ACE controller, panel, expansion, bus, pin-budget and verification architecture.

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DESIGN NOTE: The structure intentionally mirrors the control-system manual: hardware ownership, signal semantics, interfaces, failure behaviour and verification are specified separately so each can be reviewed and tested in isolation.

1. Purpose and Scope

This manual defines the physical architecture of ACE - the Arc Control Executive hardware and its human interface. It covers the Nano Every carrier, operator panel, low-voltage power domains, direct safety and real-time signals, serial buses, panel expansion, connectors, diagnostics and Revision A prototyping strategy.

The purpose is to let the control module mature while the energy-stage hardware is still being funded and developed. The ACE controller can therefore be assembled, programmed, exercised and verified against sensor simulators and low-energy fixtures before it is connected to any output stage.

- The document is authoritative for ACE hardware partitioning and interface ownership.
- The control-system and HID architecture manual remains authoritative for software behaviour.
- Energy storage, discharge switching and electrode construction are outside this manual.
- No panel bus or display function is permitted to become a single point of failure for hard inhibit or pulse termination.

2. Design Basis and Status

ACE follows the same design philosophy already adopted for the firmware: static resources, explicit ownership, bounded interfaces and a strong separation between convenience functions and the hard safety path. The hardware is intentionally modular so individual boards can be revised without changing every subsystem at once.

Design driver	Hardware consequence
Limited Nano Every I/O	Use panel expansion for slow human-interface functions.
6 KB SRAM	Avoid a permanent full OLED framebuffer where possible.
Shared I2C bus	Maintain a formal address registry and recovery policy.
Strong safety boundary	Keep trigger, grip, arm, inhibit and fault paths direct.
Long development interval	Build a standalone control-module test stack before the energy stage.
Field serviceability	Use keyed connectors, test points and replaceable daughterboards.

DESIGN NOTE: Revision A.0 is an architecture baseline. Numeric pin assignments, connector part numbers and PCB dimensions remain preliminary until the exact sensor and control modules are frozen.

3. ACE Hardware Boundary

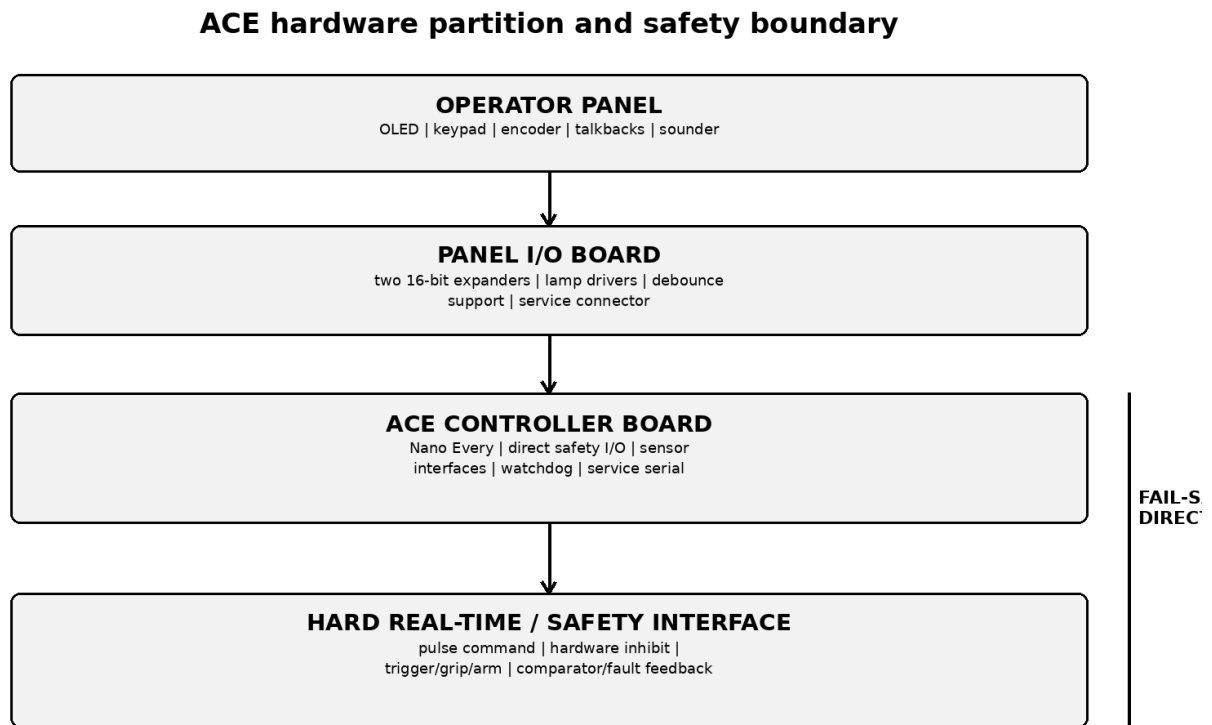


Figure 2. Hardware layers from operator panel to direct safety interface.

ACE begins at the regulated low-voltage control-power entry and ends at clearly defined command, feedback and inhibit interfaces to the rest of NanoArc. It does not own the energy path itself. The controller may request charging or a timed pulse, but independent hardware must retain authority to block or terminate unsafe action.

3.1 Included hardware

- Nano Every carrier and local support circuitry
- Panel input and output expansion
- OLED, keypad, encoder, talkbacks and sounder
- Sensor and status interfaces
- Direct trigger, grip, arm, inhibit and fault signals
- Programming, service serial and diagnostic test points

3.2 Excluded hardware

- Energy-storage bank
- High-current switching network
- Charge-converter power stage
- Electrode and work-current path
- Mains-connected supply internals

4. Target Controller Platform

The baseline controller is the Arduino Nano Every, built around the ATmega4809. The board provides a compact 45 x 18 mm module, 48 KB flash class storage, 6 KB SRAM, analog inputs, timers, serial interfaces and a familiar 5 V ecosystem. ACE treats the Nano as a replaceable processing module mounted on a carrier rather than as the entire controller assembly.

Property	Baseline use in ACE
Processor	ATmega4809 AVR at the stock 16 MHz board clock.
Program memory	Firmware, tables, diagnostics and compact profile data.
SRAM	Executive state, queues, display working data and fixed telemetry records.
I2C/TWI	Shared panel, display and sensor/control bus.
UART	Service serial and development diagnostics.
Timers	Hard real-time pulse timing and bounded scheduler support.
ADC	Voltage, current, temperature and diagnostic analog channels.

4.1 Carrier-board policy

- Socket or header-mount the Nano Every for replacement.
- Expose all direct safety signals at test points.
- Do not route high-current paths under or through the controller carrier.
- Reserve programming and USB access after installation.
- Keep spare pins and pads where practical; do not consume every resource merely because it exists.

5. Hardware Partitioning

The control module is divided into replaceable functional boards. Revision A may use perfboard or breakout modules, but the logical boundaries should match the final PCB structure from the beginning.

Assembly	Primary contents	Failure containment
ACE controller board	Nano Every, direct I/O conditioning, analog interfaces, watchdog, service header	Owens authoritative processing and direct interfaces.
Panel I/O board	Two GPIO expanders, lamp drivers, keypad/encoder connectors	Panel faults must not activate output hardware.
Operator panel	OLED, keypad, encoder, talkbacks, sounder and hard controls	Mechanical interface; replaceable without disturbing controller wiring.
Sensor/control harness board	Filtered sensor connectors and status translation	Keeps noisy or remote wiring away from the MCU carrier.

DESIGN NOTE: A second microcontroller is not part of the baseline. Panel expansion is register-based I/O, leaving command authority in ACE.

6. Power Distribution and Reset

ACE low-voltage power domains

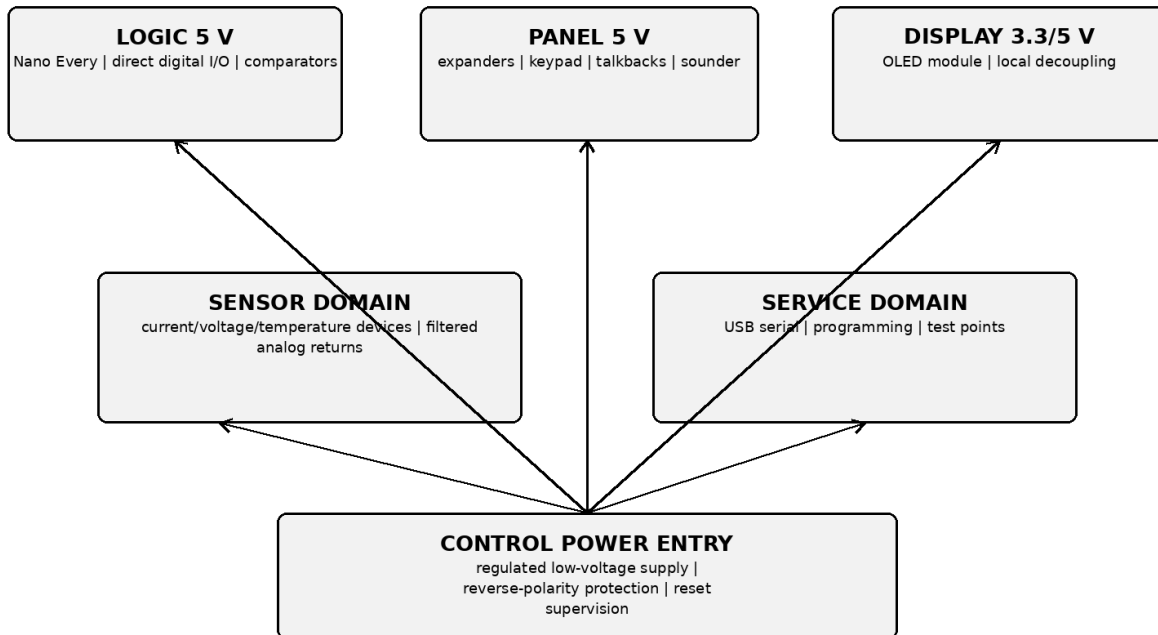


Figure 3. Proposed low-voltage ACE power domains.

ACE should receive a regulated low-voltage supply from the broader NanoArc power system. The controller carrier then distributes logic, panel, display and sensor power through locally protected branches. This avoids placing every accessory directly on the Nano Every 5 V header.

6.1 Required functions

- Reverse-polarity protection at control-power entry
- Bulk and local decoupling
- Reset supervision or brownout-aware startup
- Separate branch protection or current limiting for panel and external sensors
- Test points for each rail and ground
- Documented current budget with at least 25 percent growth margin

6.2 Reset behaviour

Any reset must leave the external inhibit asserted. Panel lamps may momentarily blank, but hardware FAULT and ENERGY indication should remain capable of asserting independently. ACE does not infer SAFE merely because the MCU has restarted.

7. Signal Classification and Ownership

Class	Examples	Routing rule
Hard real-time output	pulse command, watchdog service	Direct Nano/timer path; no panel bus.
Direct safety input	trigger, grip, arm, hard-safe, comparator fault	Direct conditioned input; interrupt or immediate sampling.
Direct control output	charge enable, hardware inhibit command	Direct output with hardware-safe default.
Measurement	voltage, current, temperature	Analog or sensor interface with plausibility checks.
Human-interface input	keypad, encoder, acknowledgement	Panel expander allowed.
Human-interface output	talkbacks, sounder, display control	Panel expander allowed, with hardware override for critical indications.
Service	UART, test mode, diagnostics	Available only under explicit service policy.

Signal classification determines where a function may be implemented. A convenient panel connection is never permitted to weaken the direct safety path.

8. Preliminary Nano Every Pin Budget

Preliminary Nano Every pin budget

Resource	Assignment	Class
D0/D1	service serial	reserved
D2	pen trigger	direct safety input
D3	grip safety	direct safety input
D4	arm switch	direct safety input
D5	hard-safe feedback	direct safety input
D6	hardware fault/comparator	direct safety input
D7	gate/output feedback	direct feedback
D8	charge-state feedback	direct feedback
D9	pulse command	hard real-time output
D10	charge enable	direct control
D11	hardware inhibit command	direct control
D12	panel interrupt	service input
D13	watchdog/service indicator	reserved
A0-A3	voltage/current/temperature	analog measurements
A4/A5	I2C SDA/SCL	shared bus
A6/A7	auxiliary analog / spare	growth

Figure 4. Preliminary direct-pin budget. Final numbering remains subject to hardware validation.

The budget demonstrates why the panel should not be wired directly to the Nano. Direct safety, feedback, analog measurement, service serial and the shared I2C bus consume nearly every sensible header resource while leaving only limited growth room.

8.1 Allocation policy

- Reserve D0/D1 for service serial during development.
- Prefer timer-capable pins for hard timing outputs.
- Keep analog channels adjacent in the carrier layout and away from noisy digital edges.
- Reserve at least one spare analog channel and one service-capable digital pad where possible.
- Do not freeze numeric assignments until timer, interrupt and peripheral conflicts are verified against the ATmega4809 core.

9. Serial Buses and Address Registry

Shared I2C bus and address registry

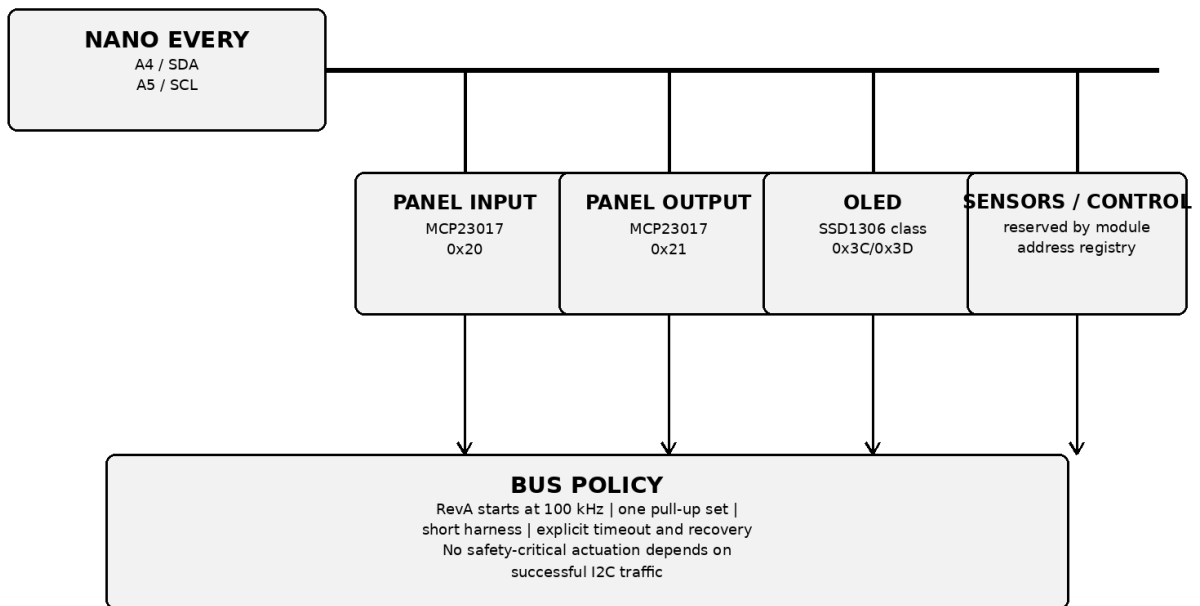


Figure 5. Shared I2C topology and address ownership.

The Nano Every exposes one practical I2C bus at the panel connector. I2C is a shared addressed bus rather than a fixed number of slots, but every attached device contributes wiring capacitance, address constraints and a possible bus-fault mechanism.

9.1 Baseline address plan

Address	Owner	Status
0x20	Panel input MCP23017	reserved
0x21	Panel output MCP23017	reserved
0x3C / 0x3D	OLED controller	module-selectable
0x40-0x4F	measurement/control modules	reserved pending module freeze
other	future devices	must be entered in registry before use

9.2 Bus rules

- Revision A starts at 100 kHz for margin and observability.
- Only one effective pull-up network is installed unless calculations justify otherwise.
- Every bus transaction has a timeout.
- The firmware includes a bus-recovery procedure before declaring the panel unavailable.
- No safety-critical action depends on successful display or panel traffic.
- A bus scanner is a service tool, not normal boot logic; required addresses are checked explicitly.

10. Operator Panel Hardware

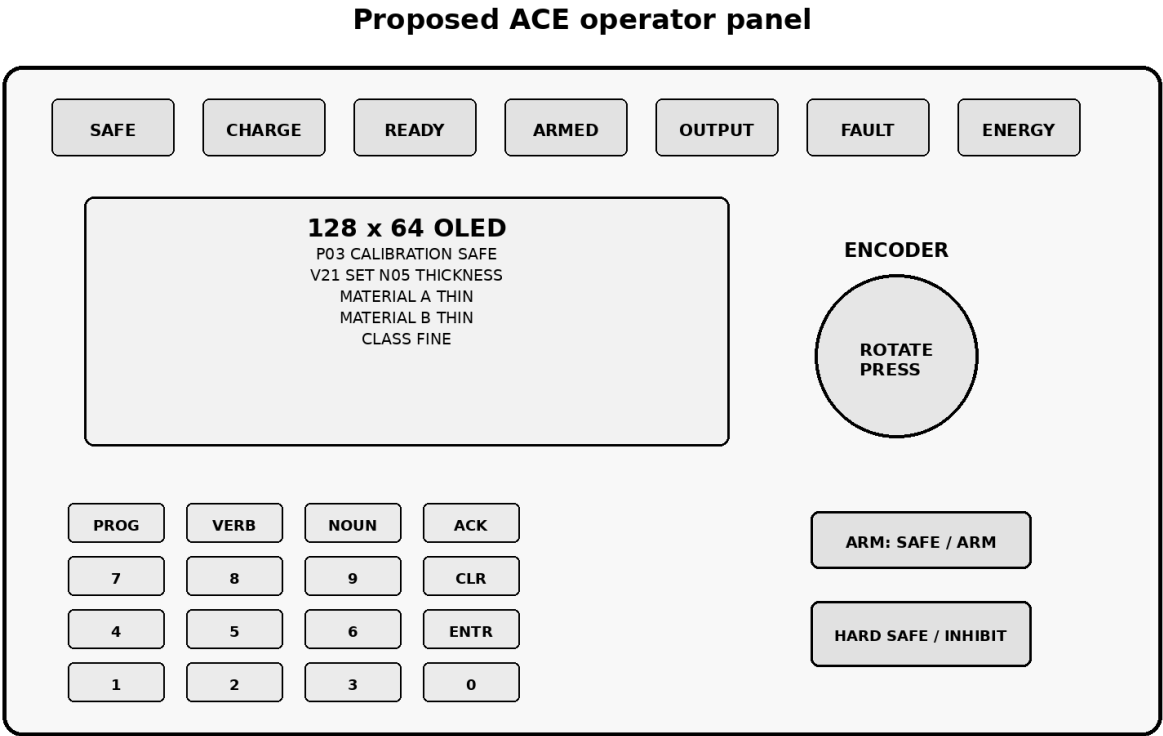


Figure 6. Proposed operator-panel arrangement.

The panel combines direct numerical command entry with a rotary encoder. This preserves the Program/Verb/Noun interaction model while making bounded adjustments and list navigation practical on a modern graphical display.

Element	Purpose
128 x 64 OLED	Contextual Program/Verb/Noun fields, monitor pages, prompts and alarms.
4 x 4 keypad	Direct Program, Verb, Noun, numeric, acknowledge, clear and enter commands.
Rotary encoder	Scrolling, bounded adjustment and field selection.
Seven talkbacks	Persistent authoritative state indication independent of page ownership.
Piezo sounder	Key acceptance, rejection and fault attention patterns.
ARM switch	Mechanically distinct maintained control; direct input.
HARD SAFE / INHIBIT	Directly asserts the hardware-safe condition and reports state to ACE.

10.1 Human-factors goals

- Readable at bench distance
- Usable with one hand while the other holds the pen
- No dependence on colour alone
- Distinct tactile form for ARM and HARD SAFE controls
- No overloaded key whose meaning changes during a critical sequence
- Critical talkbacks remain visible while the OLED displays another page

11. Keypad and Encoder

11.1 Keypad baseline

Row	Key 1	Key 2	Key 3	Key 4
1	PROG	VERB	NOUN	ACK
2	7	8	9	CLR
3	4	5	6	ENTR
4	1	2	3	0

The 4 x 4 matrix occupies eight expander pins. The scan engine must support debounce, rollover rejection and detection of impossible combinations caused by shorts or contamination. Revision A may use ordinary tactile switches; the final panel can use a custom keyplate over the same matrix.

11.2 Encoder baseline

- Quadrature A/B input plus momentary press
- Detent-based navigation rather than interrupt-per-edge command execution
- Acceleration may be added for long numeric ranges, but the final accepted value is always shown before ENTR
- Encoder press selects or enters a field; ENTR remains the unambiguous command-commit key

DESIGN NOTE: The encoder and keypad are complementary. Removing either one would simplify hardware but would make some ACE operations unnecessarily slow or ambiguous.

12. Talkbacks and Audible Indication

Talkback	Authoritative meaning	Default after reset
SAFE	Hardware and software output inhibits are asserted.	off until verified
CHARGE	The charge subsystem is actively enabled.	off
READY	Requested preconditions are satisfied.	off
ARMED	ACE has accepted the armed state.	off
OUTPUT	Pulse-output path is active.	off
FAULT	A blocking hardware or ACE fault is present.	hardware may force on
ENERGY	Stored energy is reported present.	hardware may force on

Talkbacks are labelled illuminated windows rather than anonymous LEDs. FAULT and ENERGY should accept a hardware override so they remain meaningful when the panel expander or MCU is unavailable.

12.1 Sound patterns

Pattern	Meaning
short click	key accepted
double chirp	command accepted
low short tone	command rejected
repeating attention tone	fault requires acknowledgement
continuous tone	not used in the baseline; avoid masking other sounds

13. Panel I/O Expansion

Panel I/O expansion allocation

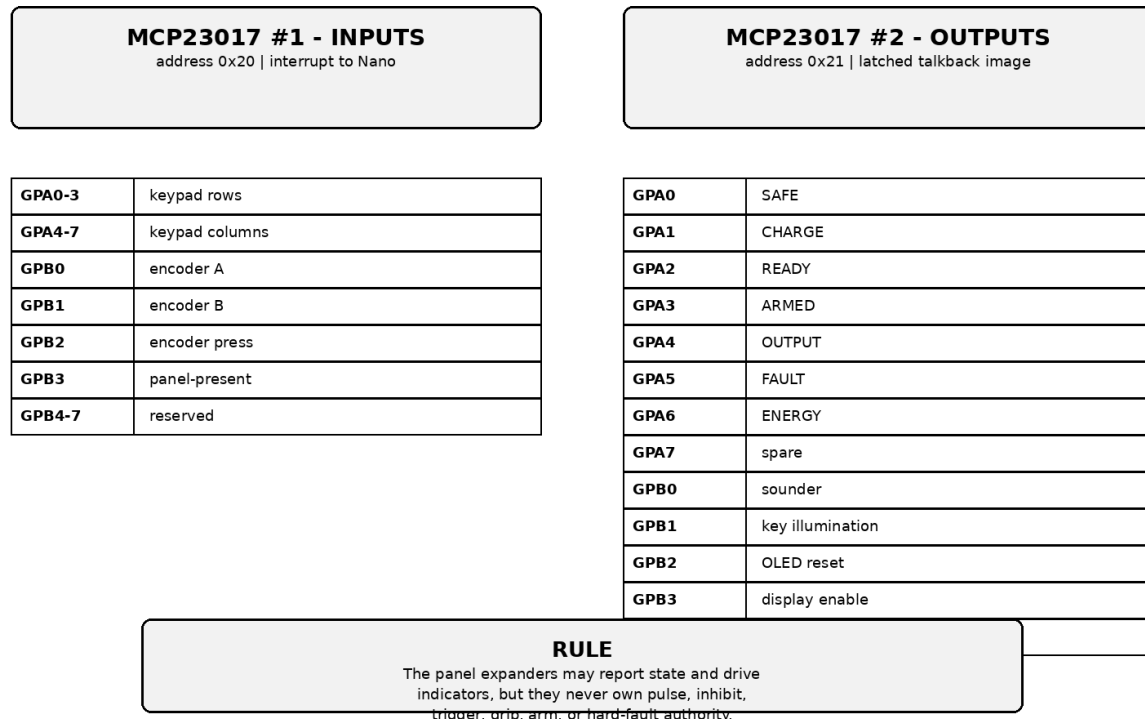


Figure 7. Two-expander panel allocation.

Two MCP23017 devices are the baseline because one device would leave no useful growth margin after keypad, encoder and seven talkbacks. Separate input and output expanders also simplify diagnostics and preserve a clean software model.

13.1 Input expander

- Scans the 4 x 4 keypad
- Reads encoder A/B and push switch
- Reports panel-present or service jumper
- Provides an interrupt output to the Nano
- Defaults all lines to inputs after reset

13.2 Output expander

- Drives a lamp-driver stage rather than panel lamps directly
- Maintains the current talkback image
- Controls the noncritical sounder and illumination
- May control OLED reset or display power
- Defaults to all outputs inactive until ACE writes a validated image

13.3 Driver stage

A transistor-array or discrete low-side driver isolates the expander from lamp current and external wiring. Current-limiting resistors belong on the panel board, and each indicator channel should have a test point or service mode.

14. Direct Safety and Real-Time Inputs

The following signals bypass the panel expanders and connect through dedicated conditioning to the Nano carrier or independent hardware. Their default electrical state must indicate safe or unavailable when a wire is open or the MCU is reset.

Signal	Direction	Required property
Pen trigger	input	direct, debounced, safe on open circuit
Grip safety	input	direct, independent from trigger
Arm switch	input	maintained and mechanically distinct
Hard-safe feedback	input	reports physical inhibit state
Hardware fault/comparator	input	latched or immediately visible
Gate/output feedback	input	detect commanded-versus-observed mismatch
Pulse command	output	timer-owned and hardware-limited
Charge enable	output	inactive on reset
Hardware inhibit command	output	asserted on reset or loss of control

DESIGN NOTE: Trigger acceptance is a system decision, not a single pin read. ACE requires the correct machine state, valid grip and arm conditions, no blocking fault and the external inhibit path available.

15. Display Hardware and Memory Impact

The baseline display is a physically larger 128 x 64 monochrome OLED module using an SSD1306-class controller. A larger panel improves readability without increasing the pixel count or command model.

15.1 Buffer strategy

A full monochrome framebuffer requires 1,024 bytes, which is a significant fraction of the Nano Every 6 KB SRAM. ACE should therefore support a page-buffered or streamed renderer unless measurement proves that a full buffer still leaves adequate worst-case stack and runtime margin.

Mode	SRAM cost	Trade-off
Full framebuffer	1,024 bytes plus library state	simplest drawing, largest fixed SRAM cost
8-row page buffer	128 bytes plus renderer state	multiple passes, strong SRAM margin
Direct text/tiles	small fixed buffers	limited graphics but highly deterministic

15.2 Display failure behaviour

- OLED absence does not block SAFE operation or diagnostics over service serial.
- The system cannot arm through a display-only prompt; physical controls and talkbacks remain authoritative.
- A display fault raises a service or operator alarm according to machine state.
- The panel remains usable for hard-safe and arm-state reporting even if OLED initialization fails.

16. Connector and Harness Architecture

ACE module and harness topology

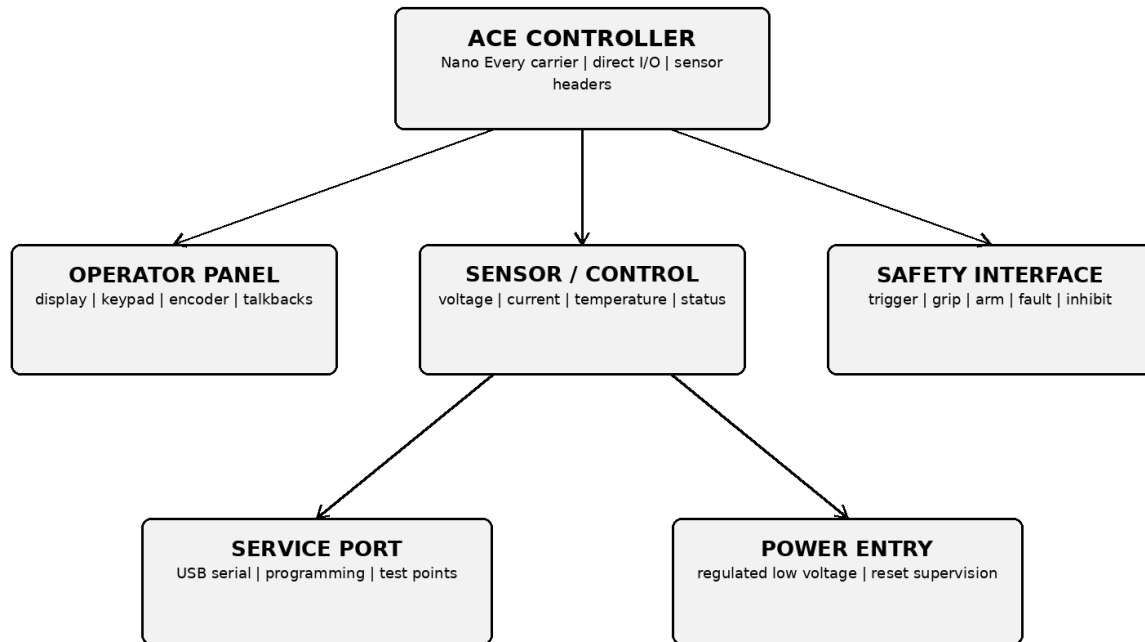


Figure 8. ACE board and harness partition.

Connectors are grouped by function and risk so a panel cable cannot be accidentally placed on a safety or sensor header. Revision A can use keyed locking headers; the final connector family remains open.

Connector group	Signals	Policy
PANEL	I2C, panel interrupt, panel power, ground	one keyed harness; no direct safety authority
SENSOR	analog and digital measurement channels	filtered, shield-aware, documented return path
SAFETY	trigger, grip, arm, hard-safe, fault, inhibit, feedback	separate keyed connector; direct signals only
SERVICE	UART, reset, test mode, optional debug pins	accessible without opening hazardous sections
POWER	regulated logic/panel supply and ground	protected entry with current budget

16.1 Harness rules

- Use separate returns for noisy loads until the controller ground point.
- Do not share talkback current with analog-sensor return conductors.
- Twist or pair remote digital inputs with ground.
- Label both ends and record pin 1 orientation.
- Provide strain relief at the panel and controller enclosure.

17. PCB and Daughterboard Strategy

The final ACE hardware should be implemented as a small stack or adjacent board set rather than one monolithic board. This keeps the Nano module replaceable and lets the operator panel evolve without touching the direct safety interface.

Board	Revision A implementation	Later implementation
Controller carrier	perfboard or prototype carrier with headers	dedicated PCB with Nano socket and direct-I/O conditioning
Panel I/O	breakout expanders plus driver board	single daughterboard behind front panel
Panel face	3D-printed or machined mockup	finished labelled faceplate and key legend
Sensor interface	terminal blocks and filter prototypes	dedicated filtered interface board

17.1 Mechanical constraints

- Keep the controller in the low-voltage compartment.
- Provide airflow without drawing conductive debris across boards.
- Orient the USB connector for service access.
- Keep the OLED and keypad replaceable from the front panel.
- Use standoffs and insulating barriers; do not rely on adhesive mounting alone.

18. EMC and Noise Resilience

NanoArc will contain fast current transitions elsewhere in the enclosure. ACE must therefore be designed as a noise-resilient control system even though it operates at low voltage.

- Keep direct safety and sensor wiring physically separated from high-current conductors.
- Use local decoupling at every IC and at each board connector.
- Filter analog channels at the receiving board and validate plausibility in firmware.
- Prefer Schmitt-trigger or comparator conditioning for long digital inputs.
- Use defined pull-ups or pull-downs so disconnected wiring fails predictably.
- Route I2C as a compact bus, not a star of long panel and sensor branches.
- Latch and report resets, brownouts and watchdog events.
- Verify that talkback or sounder switching does not disturb analog readings.

DESIGN NOTE: *The Revision A control-module test plan should include deliberately noisy switching loads and cable movement before ACE is connected to the actual energy stage.*

19. Startup Self-Test and Hardware Diagnostics

Hardware initialization and startup self-test

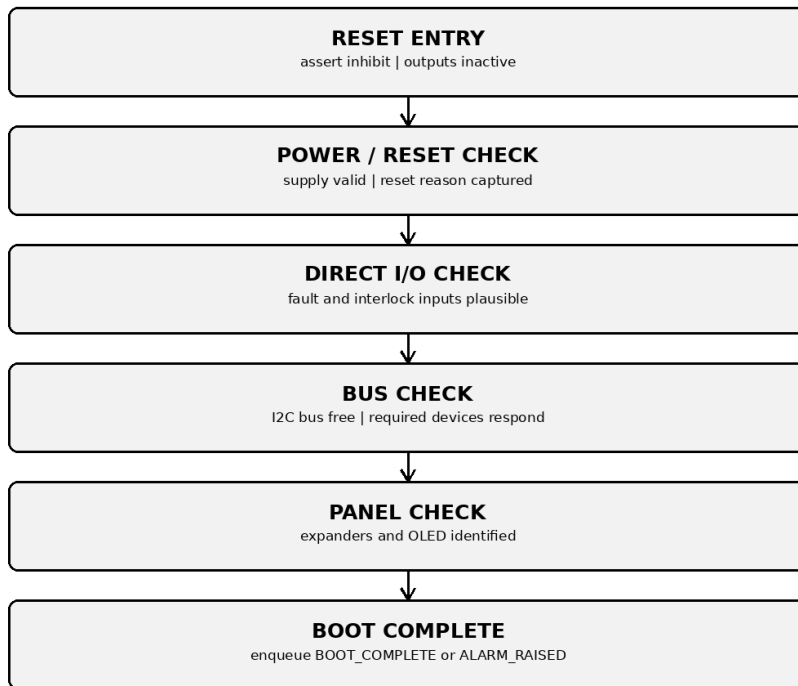


Figure 9. Proposed power-on hardware validation sequence.

Firmware setup and hardware design must agree on a deterministic startup sequence. All external commands remain inactive while ACE validates its own state, direct inputs and required peripherals.

19.1 Power-on checks

1. Assert or confirm the hardware inhibit before peripheral initialization.
2. Capture reset reason and supply status.
3. Verify direct fault and interlock inputs are electrically plausible.
4. Verify the event queue and supervisor begin in their expected state.
5. Recover and test the I2C bus.
6. Check required panel and sensor addresses individually.
7. Exercise talkback output image with a safe lamp test when permitted.
8. Enqueue BOOT_COMPLETE only after all mandatory checks pass; otherwise enqueue ALARM_RAISED.

19.2 Diagnostic observability

- Service serial prints the reset reason, missing devices and pin states.
- Test points expose bus, reset, inhibit and major power rails.
- Panel service mode can test keys, encoder and lamps without enabling control outputs.
- Fault history distinguishes hardware absence, implausible input and communication timeout.

20. Serviceability and Revision Management

ACE is expected to evolve over several hardware revisions. The module therefore needs explicit identity and configuration rather than relying on visual inspection of hand wiring.

- Assign board IDs and revision markings to controller and panel boards.
- Store the expected panel and sensor configuration in firmware tables.
- Record I2C addresses, connector pinouts and jumper settings in this manual.
- Use a service header or EEPROM/strap method if future boards require automatic identification.
- Do not silently repurpose a connector pin between revisions; mark incompatible changes.

20.1 Recommended labels

Label	Example
Controller board	ACE-CTRL-A0
Panel I/O board	ACE-PANEL-A0
Harness	ACE-HARNESS-P1
Firmware compatibility	ACE FW A-series
Document	NA-ACEHW-001

21. Revision A Prototype Plan

Revision A control-module development stack

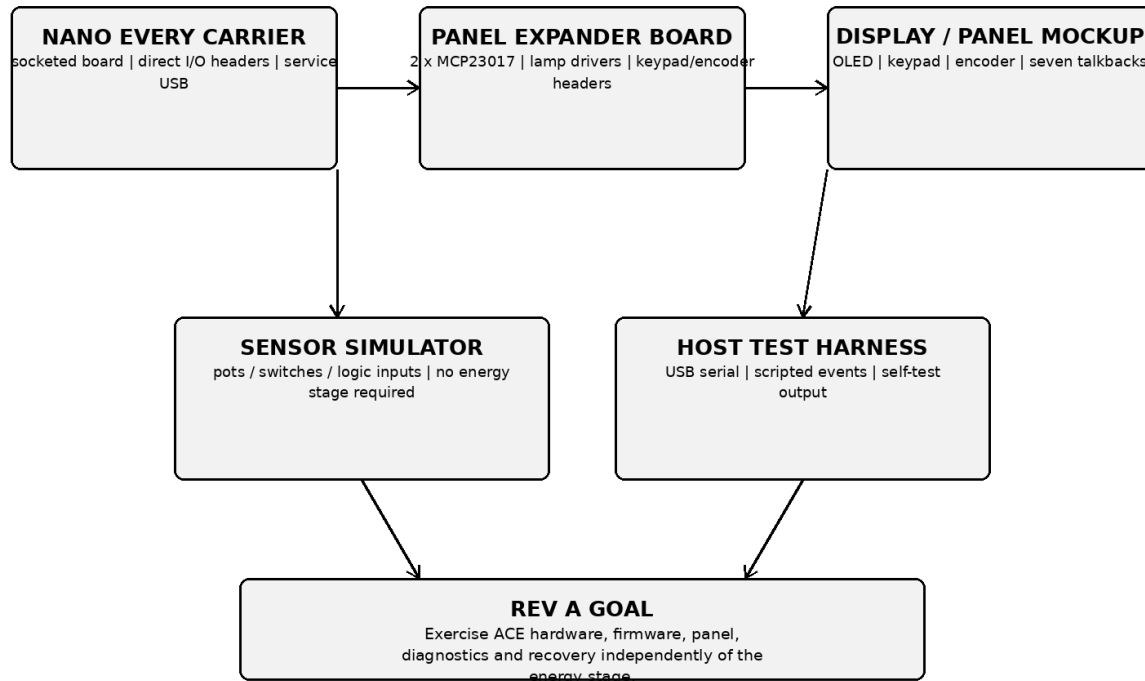


Figure 10. Standalone Revision A control-module development arrangement.

The control module can make meaningful progress without the energy-stage hardware. Revision A should therefore be treated as a complete development target rather than a temporary wiring exercise.

21.1 Prototype stages

1. Nano Every carrier with safe defaults, service serial and direct-I/O headers.
2. Panel I/O board with one expander, then two expanders.
3. OLED and keypad/encoder mockup.
4. Talkback driver board and lamp-test mode.
5. Sensor simulator using switches and low-voltage analog sources.
6. Startup self-test, fault injection and bus-recovery testing.
7. Enclosure and harness mockup.
8. Only after control-module acceptance: connect to separately verified external hardware interfaces.

21.2 Exit criteria

- All panel keys and encoder actions are detected without phantom events.
- Every talkback can be commanded and independently verified.
- I2C bus lockup is detected and handled without unsafe state change.
- Resets always return to inhibited operation.
- Direct safety inputs override panel commands.
- Host tests and Nano cross-build remain nominal.
- Pin assignments, addresses and connectors are frozen for the next revision.

22. Preliminary Bill of Materials

Item	Qty	Role	Status
Arduino Nano Every	1	controller module	selected
Nano carrier/prototype board	1	controller assembly	TBD
MCP23017	2	panel input/output expansion	baseline
ULN2803A or equivalent driver	1	talkback/sounder low-side drive	baseline
128 x 64 OLED, large physical format	1	operator display	controller/module TBD
4 x 4 keypad or 16 tactile switches	1	command entry	baseline
EC11-class rotary encoder with push	1	navigation and value editing	baseline
labelled talkback windows / LEDs	7	state indication	mechanical TBD
piezo sounder	1	audible feedback	baseline
maintained ARM switch	1	direct operator control	mechanical TBD
hard-safe/inhibit control	1	direct safety control	mechanical TBD
locking connectors and harness parts	set	panel, sensor, safety and power groups	TBD
decoupling, pull-ups, resistors, protection	set	support circuitry	values after schematic

DESIGN NOTE: This list is for ACE low-voltage hardware only. It intentionally excludes energy-storage and output-stage components.

23. Verification and Acceptance

Test group	Minimum evidence
Power and reset	measured rails, brownout/reset capture, safe defaults
Direct I/O	open/closed/short simulation and expected state
Panel inputs	every key, encoder direction, debounce and rollover rejection
Panel outputs	each talkback, sounder and OLED control
I2C	address scan, required-device checks, timeout and recovery
Analog interfaces	range, noise, filtering and plausibility limits
Firmware integration	startup path, event queue, supervisor and alarms
EMC/noise	switching-load and cable-disturbance tests
Serviceability	connector keying, labels, test-point access and board replacement

23.1 Acceptance records

- Firmware commit and build summary
- Board and harness revision identifiers
- Pin and address tables
- Measured idle and worst-case current
- Fault-injection results
- Known deviations and open decisions

24. Open Decisions

Decision	Current baseline	Needed evidence
OLED module	large 128 x 64 monochrome	physical module, interface and memory test
Panel expander interface	two MCP23017 on shared I2C	bus robustness with actual sensor modules
Talkback driver	ULN2803A-class low-side array	lamp current and voltage choice
Panel connector	single keyed low-voltage harness	pin count, availability and enclosure geometry
Hard-control hardware	distinct maintained ARM and hard-safe controls	mechanical selection and fail-safe contact arrangement
Display buffer	page-buffered preferred	measured SRAM and update latency
Direct pin numbering	preliminary only	timer/interrupt/core validation
Sensor addresses	reserved registry range	final module selection

Each decision should be closed by test evidence or a clearly documented constraint. A purchasing decision alone is not sufficient to freeze an interface.

Appendix A. Preliminary Pin Assignment

Pin	Proposed use	Ownership	Notes
D0	service RX	service	reserve during development
D1	service TX	service	reserve during development
D2	pen trigger	direct safety	conditioned input
D3	grip safety	direct safety	conditioned input
D4	arm switch	direct safety	maintained input
D5	hard-safe feedback	direct safety	safe on open
D6	hardware fault/comparator	direct safety	interrupt capable preferred
D7	gate/output feedback	direct feedback	mismatch detection
D8	charge-state feedback	direct feedback	optional by charger design
D9	pulse command	hard real-time	timer-owned
D10	charge enable	direct control	inactive on reset
D11	hardware inhibit command	direct control	asserted on reset
D12	panel interrupt	panel service	open-drain input
D13	watchdog/service indicator	reserved	subject to onboard LED interaction
A0	bank/input voltage	measurement	divider/filter external
A1	supply current	measurement	sensor dependent
A2	output/bank current	measurement	sensor dependent
A3	power-stage temperature	measurement	sensor dependent
A4	I2C SDA	shared bus	panel/display/sensors
A5	I2C SCL	shared bus	panel/display/sensors
A6	aux temperature	measurement	growth
A7	spare analog	reserve	do not consume without review

Appendix B. I2C Address Registry

7-bit address	Device class	Owner/status	Notes
0x20	GPIO expander	panel input / reserved	A2:A0 = 000
0x21	GPIO expander	panel output / reserved	A2:A0 = 001
0x22-0x27	GPIO expansion	future / reserved	requires document update
0x3C	OLED	preferred	common SSD1306-class address
0x3D	OLED	alternate	module-dependent
0x40-0x4F	measurement/control	reserved range	actual modules TBD
other	unassigned	prohibited until registered	check fixed-address conflicts

DESIGN NOTE: This registry is an ACE project policy, not a statement that every device can select any listed address. Module datasheets remain authoritative.

Appendix C. Talkback Behaviour

State/event	SAFE	CHARGE	READY	ARMED	OUTPUT	FAULT	ENERGY
reset / unknown	off	off	off	off	off	HW	HW
SAFE verified	on	off	off	off	off	off	state
charging	off	on	off	off	off	off	on
ready	off	off	on	off	off	off	on
armed	off	off	state	on	off	off	on
output active	off	off	off	on	on	off	on
fault	state	off	off	off	off	on	state

HW means the indicator may be asserted by hardware independently of the panel output image. State means the indication depends on measured system condition rather than on the machine-state name alone.

Appendix D. Connector Register

Connector	Pins	Provisional signals	Status
J1 CONTROL POWER	TBD	regulated supply, ground, optional power-good	open
J2 PANEL	TBD	5 V, ground, SDA, SCL, panel IRQ, optional reset	open
J3 SAFETY	TBD	trigger, grip, arm, hard-safe, fault, inhibit, feedback	open
J4 SENSORS	TBD	analog and digital measurement channels	open
J5 SERVICE	TBD	UART, reset, test mode, ground	open

DESIGN NOTE: Connector pin numbering is intentionally withheld until the schematic and physical connector family are selected. Keying and safe mating behaviour are required acceptance criteria.

References

1. Arduino. Arduino Nano Every (ABX00028) official datasheet and hardware documentation.
2. Microchip Technology. MCP23017/MCP23S17 16-Bit I/O Expander with Serial Interface, DS20001952.
3. STMicroelectronics. ULN2801A, ULN2802A, ULN2803A and ULN2804A transistor-array datasheet.
4. Solomon Systech. SSD1306 128 x 64 monochrome OLED driver product documentation.
5. NanoArc. Control System and Human-Interface Architecture Manual, Revision A.
6. Virtual AGC Project. Virtual AGC Assembly-Language Manual and source-derived interface references.

DESIGN NOTE: *Where this manual conflicts with a component manufacturer datasheet, the manufacturer datasheet controls the electrical design. Where it conflicts with the NanoArc control-system manual, the conflict must be resolved and both documents revised before implementation.*